IEEE SSCS/CASS Atlanta Joint Chapter Seminar

Title: How to live with Statistical Variations the "Neuromorphic" way

Speaker: Arindam Basu, Assistant Professor
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Abstract: As CMOS technology has been scaling down over the last decade, the effect of statistical variations (or component mismatch) and their impact on circuit design have become increasingly prominent. In this talk, I will present some of the work done by our group where we take inspiration from neuroscience and show new approaches to perform machine learning with low-energy consumption using low-resolution mismatched components. First, I will talk about "combinatoric learning" using binary synapses—an alternative to weight based learning in neural networks. Second, I will present an example of utilizing component mismatch to perform part of the computation—an example of algorithm-hardware co-design. Lastly, I will show an application of such a low-power machine learner to perform intention decoding in brain-machine interfaces.

Speaker Biography: Arindam Basu received the B.Tech and M.Tech degrees in Electronics and Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur, in 2005, and the M.Sc. degree in Mathematics and the Ph.D. degree in Electrical and Computer Engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2009 and 2010, respectively. In June 2010, he joined Nanyang Technological University, Singapore, as an Assistant Professor. His research interests include bio-inspired neuromorphic circuits, non-linear dynamics in neural systems, low power analog IC design, and programmable circuits and devices.

Dr. Basu received the JBNSTS Award in 2000 and the Prime Minister of India Gold Medal in 2005 from the Indian Institute of Technology, Kharagpur. He received the best student paper award, Ultrasonics Symposium, 2006; best live demonstration, ISCAS 2010; and a finalist position in the best student paper contest at ISCAS 2008. He was awarded MIT Technology Reviews inaugural TR35@ Singapore award in 2012 for being among the top 12 innovators under the age of 35 in SE Asia, Australia, and New Zealand.

Seminar Time: 12:00PM-1:00PM on Oct 26th 2015

Seminar Location: TSRB 509 GEDC Board Room, Georgia Tech.

Organizer: Dr. Hua Wang, IEEE SSCS/CASS Atlanta Joint Chapter Chair, Assistant Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology. Email: hua.wang@ece.gatech.edu. Phone: (404) 385-6003

Light refreshments will be served at the seminar.