



IEEE SSCS/CASS Atlanta Joint Chapter Seminar

DTC-Based Digital PLLs

Speaker: Professor Carlo Samori

Affiliation: Department of Electronics, Information, and Bioengineering,
Politecnico di Milano, Italy

Abstract: Digital phase-locked loops (DPLLs) have emerged in last ten years as an important alternative to analog PLLs, also for fractional-N synthesis in wireless applications where a very demanding spectral purity is required. While in the initial implementations the key building block of DPLLs was a multibit time to digital converter (TDC), which is power consuming circuit analog to an ADC, record performance have been ultimately obtained by exploiting an architecture featuring a time arbiter, i.e. a single-bit TDC, driven by a multi bit digital-to-time converter (DTC). The key enabling idea is to exploit the dithering property of the thermal noise always present in a circuit.



The presentation reviews the path that has led to this approach, which epitomize how scaled CMOS technologies may enable powerful calibration techniques achieving unprecedented performance.

Speaker Biography: Carlo Samori received the Ph.D. in electrical engineering in 1995, from the Politecnico di Milano, Italy, where he is now a professor.

His research interests are in the area of RF circuits, in particular of design and analysis of VCOs and high performance frequency synthesizers. He has collaborated with several semiconductor companies. He is a co-author of more than 100 papers and of the book *Integrated Frequency Synthesizers for Wireless Systems* (Cambridge University Press, 2007). Prof. Samori has been a member of the Technical Program Committee (TPC) of the IEEE International Solid-State Circuits Conference and he is a member of the TPC of the European Solid-State Circuits Conference. He has been Guest Editor for the December 2014 issue of the Journal of Solid-State Circuits.

Carlo Samori is a Distinguished Lecturer of the IEEE Solid-State Circuits Society and an IEEE Fellow.

Seminar Time: 10:30AM-11:30AM on November 13th 2017 **Seminar Location:** TSRB 509, Georgia Tech

Organizer: Dr. Hua Wang, IEEE SSCS/CASS Atlanta Joint Chapter Chair, Assistant Professor, School of ECE, Georgia Technology. Email: hua.wang@ece.gatech.edu. Phone: (404) 385-6003