



## IEEE SSCS Distinguished Lecture

### IEEE SSCS/CASS Atlanta Joint Chapter Seminar

**Title:** Low-Power, High-Bandwidth, and Ultra-Small Memory Module Design

**Speaker:** Professor Russell Jacob (Jake) Baker (Department of Electrical Engineering)

**Affiliation:** University of Nevada, Las Vegas, Nevada, USA

**Abstract:** This work proposes a novel DRAM module and interconnect architectures in an attempt to improve computing energy use and performance. A low cost advanced packaging technology is used to propose an 8 die and 32-die memory module. The 32-die memory module measures less than  $2 \text{ cm}^3$ . The size and packaging technique allow the memory module to consume less power than conventional module designs. A 4 Gb DRAM architecture utilizing 64 data pins is proposed. The DRAM architecture is inline with ITRS roadmaps and can consume 50% less power while increasing bandwidth by 100%. The large number of data pins are supported by a low power capacitive-coupled interconnect. The receivers developed for the capacitive interface were fabricated in  $0.5 \mu\text{m}$  and  $65 \text{ nm}$  CMOS technologies. The  $0.5 \mu\text{m}$  design operated at 200 Mbps, used a coupling capacitor of 100 fF, and consumed less than 3 pJ/bit of energy. The  $65 \text{ nm}$  design operated at 4 Gbps, used a coupling capacitor of 15 fF, and consumed less than 15 fJ/bit and order of magnitude smaller consumptions than previously reported receiver designs.

**Speaker Biography:** Professor Russel Jacob Baker received the B.S. and M.S. degrees in Electrical Engineering from the University of Nevada, Las Vegas in 1986 and 1988, respectively, and the Ph.D. degree in Electrical Engineering from the University of Nevada, Reno in 1993. He is currently a full Professor at the Department of Electrical and Computer Engineering, University of Nevada, Las Vegas.

Professor Baker holds over 200 granted or pending patents in integrated circuit design. He is a member of the electrical engineering honor society Eta Kappa Nu, a licensed Professional Engineer, a popular lecturer that has delivered over 50 invited talks around the world, an IEEE Fellow, and the author of the books CMOS Circuit Design, Layout, and Simulation, CMOS Mixed-Signal Circuit Design, and a coauthor of DRAM Circuit Design: Fundamental and High-Speed Topics. He received the Best Paper Award from the IEEE Power Electronics Society in 2000, the Frederick Emmons Terman Award in 2007, and the IEEE Circuits and Systems (CAS) Education Award in 2011.

Professor Baker currently serves, or has served, on the IEEE Press Editorial Board (1999-2004), as a member of the first Academic Committee of the State Key Laboratory of Analog and Mixed-Signal VLSI at the University of Macau (2007-present), as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-present), on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016), as an Advisory Professor to the School of Electronic and Information Engineering at Beijing Jiaotong

University (2012-present), as the Technology Editor for the IEEE Solid-State Circuits Magazine (2012-present), and as a Distinguished Lecturer for the SSCS (2013-present).

**Seminar Time:** 2:00PM-3:30PM on April 4<sup>th</sup> 2014

**Seminar Location:** Technology Square Research Building (TSRB), 1st Floor Auditorium (Rm118), 85 5th Street NW, Atlanta, GA 30308

**Organizer:** Dr. Hua Wang, IEEE SSCS/CASS Atlanta Joint Chapter Chair, Assistant Professor, School of Electrical and Computer Engineering, Georgia Institute of Technology.

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**Light refreshments will be served at the seminar.**